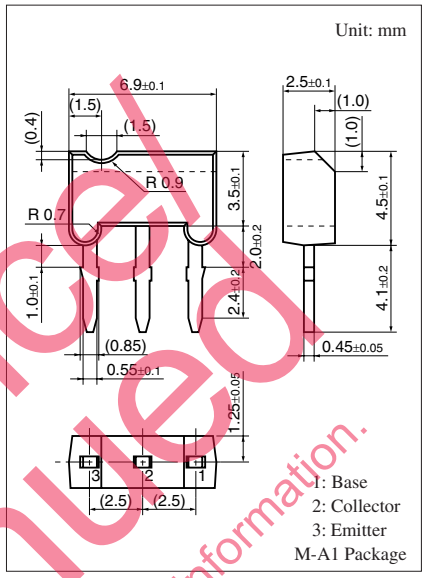
2SD1350, 2SD1350A

Silicon NPN triple diffusion planar type

For high breakdown voltage switching



■ Features

- High collector-base voltage (Emitter open) V_{CBO}
- Large collector power dissipation P_C
- Low collector-emitter saturation voltage $V_{CE(sat)}$
- M type package, allowing easy automatic and manual insertion as well as stand-alone fixing to the printed circuit board.

■ Absolute Maximum Ratings $T_a = 25°C$

Parameter		Symbol	Rating	Unit
Collector-base voltage (Emitter open)	2SD1350	V_{CBO}	400	V
	2SD1350A		600	
Collector-emitter voltage (Base open)	2SD1350	V_{CEO}	400	V
	2SD1350A		500	
Emitter-base voltage (Collector open)		V_{EBO}	5	V
Collector current		I_C	500	mA
Peak collector current		I_{CP}	1	A
Collector power dissipation *		P_C	1	W
Junction temperature		T_j	150	°C
Storage temperature		T_{stg}	−55 to +150	°C

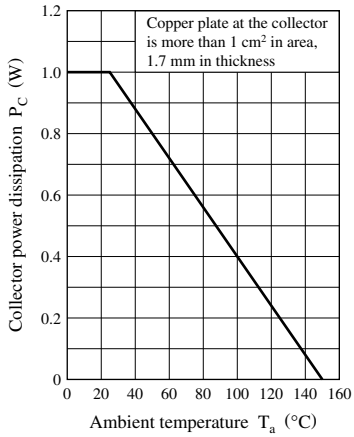
Note) ∗: Printed circuit board: Copper foil area of 1 cm² or more, and the board thickness of 1.7 mm for the collector portion

■ Electrical Characteristics $T_a = 25°C \pm 3°C$

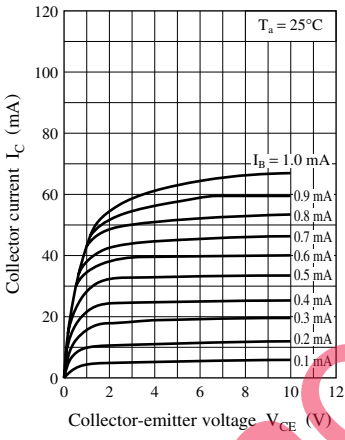
Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Collector-base voltage (Emitter open)	2SD1350	V_{CBO}	I_C = 100 µA, I_E = 0	400			V
	2SD1350A			600			
Collector-emitter voltage (Base open)	2SD1350	V_{CEO}	I_C = 500 µA, I_B = 0	400			V
	2SD1350A			500			
Emitter-base voltage (Collector open)		V_{EBO}	I_E = 100 µA, I_C = 0	5			V
Forward current transfer ratio		h_{FE}	V_{CE} = 5 V, I_C = 30 mA	30			—
Collector-emitter saturation voltage		$V_{CE(sat)}$	I_C = 250 mA, I_B = 50 mA			1.5	V
Base-emitter saturation voltage		$V_{BE(sat)}$	I_C = 250 mA, I_B = 50 mA			1.5	V
Transition frequency		f_T	V_{CB} = 30 V, I_E = −20 mA, f = 200 MHz		55		MHz
Collector output capacitance (Common base, input open circuited)		C_{ob}	V_{CB} = 30 V, I_E = 0, f = 1 MHz			7	pF
Turn-on time		t_{on}	V_{CC} = 200 V, I_C = 100 mA I_{B1} = 10 mA, I_{B2} = −10 mA		0.4		µs
Fall time		t_f	V_{CC} = 200 V, I_C = 100 mA I_{B1} = 10 mA, I_{B2} = −10 mA		0.7		µs
Storage time		t_{stg}	V_{CC} = 200 V, I_C = 100 mA I_{B1} = 10 mA, I_{B2} = −10 mA		3.6		µs

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

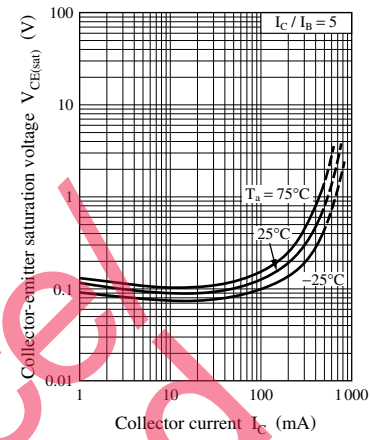
P_C — T_a



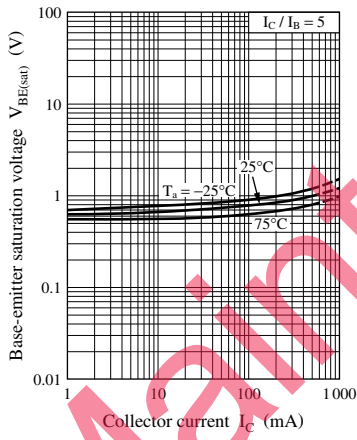
I_C — V_{CE}



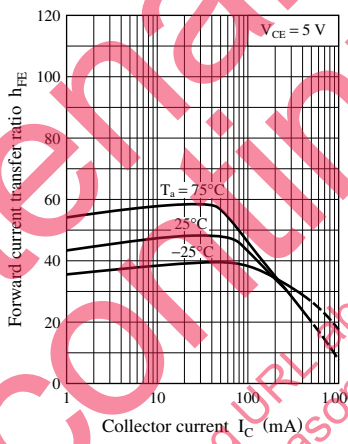
$V_{CE(sat)}$ — I_C



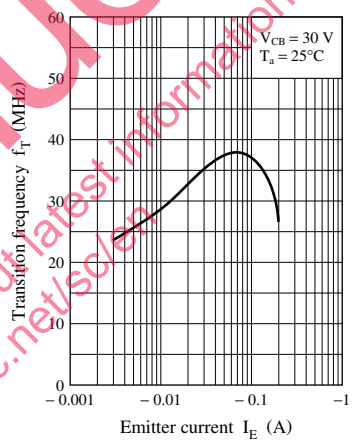
$V_{BE(sat)}$ — I_C



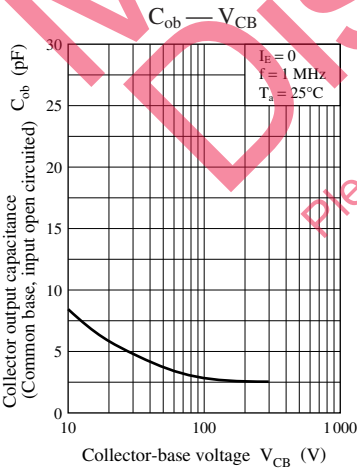
h_{FE} — I_C



f_T — I_E



C_{ob} — V_{CB}



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